Henry (Hank) Hoffmann

CONTACT INFORMATION

Computer Science and Artificial Intelligence Laboratory
Massachusetts Institute of Technology
MIT CSAIL
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Cambridge, MA 02139 USA

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OBJECTIVE

An academic faculty position leading research in multicore and parallel computing.

- More information and auxiliary documents can be found at `http://people.csail.mit.edu/hank`

CITIZENSHIP

USA

RESEARCH INTERESTS

My goal is holistic design of computer applications, system software, and architecture for parallel computing. I am especially motivated by the development of *self-adaptive*, or *autonomic* techniques, which enable system software and hardware to self-tune and meet application goals optimally while responding to unforeseen events. I have been conducting research in parallel computing for 12 years and multicore for 10 years.

EDUCATION

Massachusetts Institute of Technology, Cambridge, MA USA

Ph.D., Electrical Engineering and Computer Science, October 2012

- Thesis: *SEEC: A framework for Self-Aware Computing*
- Adviser: Professor Anant Agarwal
- Committee: Professor Srinivas Devadas, Professor Alan Edelman
- Minor: Geometry

S.M., Electrical Engineering and Computer Science, June 2003

- Thesis: *Stream Algorithms and Architecture*
- Adviser: Professor Anant Agarwal

University of North Carolina at Chapel Hill

B.S. with Highest Honors and Highest Distinction,
Mathematical Sciences, May 1999

- Computer Science Concentration

CONFERENCE, WORKSHOP, & JOURNAL PUBLICATIONS

M. Maggio, H. Hoffmann, A. V. Papadopoulos, J. Panerati, M. D. Santambrogio, A. Agarwal, A. Leva. Comparison of Decision Making Strategies in Autonomic Computing. To appear in *ACM Transactions on Autonomic and Adaptive Systems.*

H. Hoffmann, A. Agarwal, S. Devadas. Selecting Spatiotemporal Patterns for Development of Parallel Applications. To appear in *IEEE Transactions on Parallel and Distributed Systems.*

M. Maggio, H. Hoffmann, M. D. Santambrogio, A. Agarwal, A. Leva. Power optimization in embedded systems via feedback control of resource allocation. To appear in *IEEE Transactions on Control Systems Technology.*

Jim Holt, Henry Hoffmann. SEEC-AP: Self-Aware Software Architecture Patterns. In *the 2nd International Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments*, June 2012.

Henry Hoffmann, Jim Holt, George Kurian, Eric Lau, Martina Maggio, Jason E. Miller, Sabrina M. Neuman, Mahmut E. Sinangil, Yildiz Sinangil, Anant Agarwal, Anantha P. Chandrakasan, Srinivas Devadas. Self-aware Computing in the Angstrom Processor. In *the 49th Annual Design Automation Conference (DAC)*, June, 2012.

Filippo Sironi, Davide B. Bartolini, Simone Campanoni, Fabio Cancare, Henry Hoffmann, Donatella Sciuto, Marco D. Santambrogio. Metronome: operating system level performance management via self-adaptive computing. In *the 49th Annual Design Automation Conference (DAC)*, June, 2012.

O. Khan, H. Hoffmann, M. Lis, F. Hijaz, A. Agarwal, S. Devadas, ARCc: A Case for an Architecturally Redundant Cache-coherence Architecture for Large Multicores. In *29th IEEE International Conference on Computer Design*, October, 2011

S. Sidiroglou, S. Misailovic, H. Hoffmann, M. Rinard. Managing Performance vs. Accuracy Trade-offs With Loop Perforation. In *ACM SIGSOFT Symposium on the Foundations of Software Engineering*, September 2011.

M. Maggio, H. Hoffmann, M. D. Santambrogio, A. Agarwal, and A. Leva Decision Making in Autonomic Computing Systems: Comparison of Approaches and Techniques. In *8th IEEE/ACM International Conference on Autonomic Computing and Communications,* June 2011.

M. Maggio, H. Hoffmann, A. Agarwal, and A. Leva Control-theoretical CPU allocation: Design and Implementation with Feedback Control. In *6th International Workshop on Feedback Control Implementation and Design in Computing Systems and Networks,* June 2011.

H. Hoffmann, S. Sidiroglou, M. Carbin, S. Misailovic, A. Agarwal, M. Rinard. Dynamic Knobs for Responsive Power-Aware Computing. In *Proceedings of the 15th International Conference on Architectural Support for Programming Languages and Operating Systems*, March 2011.

M. Maggio, H. Hoffmann, M. D. Santambrogio, A. Agarwal, and A. Leva. Controlling software applications via resource allocation within the Heartbeats frame work. In *49th IEEE Conference on Decision and Control*, pages 3736 –3741, December 2010.

M. Rinard, H. Hoffmann, S. Misailovic, S. Sidiroglou. Patterns and statistical analysis for understanding reduced resource computing. In *Proceedings of the ACM international conference on Object oriented programming systems languages and applications*, October 2010.

F. Sironi, M. Triverio, H. Hoffmann, M. Maggio, M. D. Santambrogio. Self-Aware Adaptation in FPGA-based Systems. In *International Conference on Field Programmable Logic and Applications*, pages 187 –192, September 2010.

H. Hoffmann, J. Eastep, M. D. Santambrogio, J. E. Miller, and A. Agarwal. Application Heartbeats: A Generic Interface for Specifying Program Performance and Goals in Autonomous Computing Environments. In *7th International Conference on Autonomic Computing*, June 2010.

M. D. Santambrogio, H. Hoffmann, J. Eastep, A. Agarwal. Enabling technologies for self-aware adaptive systems. In *NASA/ESA Conference on Adaptive Hardware and Systems*, pages 149–156, June 2010.

J. Psota, J. E. Miller, G. Kurian, H. Hoffmann, N. Beckmann, J. Eastep, A. Agarwal. ATAC: Improving performance and programmability with on-chip optical networks. In *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pages 3325–3328, June 2010.

S. Misailovic, S. Sidiroglou, H. Hoffmann, M. C. Rinard. Quality of service profiling. In *Proceedings of the 32nd ACM/IEEE International Conference on Software Engineering*, pages 25-34, May 2010.

H. Hoffmann, S. Devadas, A. Agarwal. A Pattern for Efficient Parallel Computation on Multicore Processors with Scalar Operand Networks. In *2nd Annual Conference on Parallel Programming Patterns*, March 2010.

H. Hoffmann, D. Wentzlaff, A. Agarwal. Remote Store Programming. In *High Performance Embedded Architectures and Compilers*, pages 3–17, January 2010.

H. Hoffmann, J. Eastep, M. D. Santambrogio, J. E. Miller, A. Agarwal. Application Heartbeats: A Generic Interface for Expressing Performance Goals and Progress in Self-Tuning Systems. In *4th Workshop on Statistical and Machine learning approaches to ARchitecture and compilaTion*, January 2010.

H. Hoffmann, J. Eastep, M. D. Santambrogio, J. E. Miller, A. Agarwal. Application heartbeats for software performance and health. In *Proceedings of the 15th ACM SIGPLAN symposium on Principles and practice of parallel programming (PPoPP 2010)*, pages 347–348, January 2010.

H. Hoffmann, A. Agarwal, S. Devadas. Partitioning Strategies: Spatiotemporal Patterns of Program Decomposition. In *Proceedings of the 21st International Conference on Parallel and Distributed Computing and Systems*, November, 2009.

H. Hoffmann, D. Wentzlaff, A. Agarwal. Remote Store Programming: Reflective Memory for Multicore. In *High Performance Embedded Computing Workshop*, September 2009.

H. Hoffmann, A. Agarwal, S. Devadas. Partitioning strategies for concurrent programming. In *1st Annual Conference on Parallel Programming Patterns*, June 2009.

D. Wentzlaff, P. Griffin, H. Hoffmann, L. Bao, B. Edwards, C. Ramey, M. Mattina, C. Miao, J. F. Brown III, A. Agarwal. On-Chip Interconnection Architecture of the Tile Processor. *IEEE Micro* vol. 27, no. 5, pages 15–31, 2007.

M. Drake, H. Hoffmann, R. M. Rabbah, S. P. Amarasinghe. MPEG-2 decoding in a stream programming language. In *20th International Parallel and Distributed Processing Symposium*, April 2006.

N. Travinin, H. Hoffmann, R. Bond, H. Chan, J. Kepner, E. Wong. pMapper: Automatic Mapping of Parallel MATLAB Programs. In *High Peformance Embedded Computing Workshop*, September 2005.

N. Travinin, H. Hoffmann, R. Bond, H. Chan, J. Kepner, E. Wong. Automatic Parallelization with pMapper. In *Cluster Computing*, pages 1–2, September, 2005.

N. Travinin, H. Hoffmann, R. Bond, H. Chan, J. Kepner, E. Wong. pMapper: Automatic Mapping of Parallel MATLAB Programs. In *DOD HPCMP (High Performance Computing Modernization Program) Users Group Conference*, pages 254–261, June 2005.

J. Lebak, J. Kepner, H. Hoffmann, E. Rutledge. Parallel VSIPL++: An Open Standard Software Library for High-Performance Parallel Signal Processing. In *Proceedings of the IEEE*, vol.93, no.2, pp.313-330, Feb. 2005

V. Strumpen, H. Hoffmann, A. Agarwal. Stream Algorithms and Architecture. In *The Journal of Instruction-Level Parallelism*, vol. 6, September 2004.

H. Hoffmann, J. Lebak. Mapping Signal Processing Kernels to Tiled Architectures. In *High Peformance Embedded Computing Workshop*, September 2004.

M. B. Taylor, W. Lee, J. E. Miller, D. Wentzlaff, I. Bratt, B. Greenwald, H. Hoffmann, P. Johnson, J. S. Kim, J. Psota, A. Saraf, N. Shnidman, V. Strumpen, M. Frank, S. P. Amarasinghe, A. Agarwal. Evaluation of the Raw Microprocessor: An Exposed-Wire-Delay Architecture for ILP and Streams. In *International Symposium on Computer Architecture*, pages 2–13, June 2004.

J. Lebak, H. Hoffmann, J. McMahon. Kernel Benchmarks and Metrics for Polymorphous Computer Architectures. In *High Peformance Embedded Computing Workshop*, September 2003.

M. B. Taylor, J. Kim, J. Miller, D. Wentzlaff, F. Ghodrat, B. Greenwald, H. Hoffmann, P. Johnson, W. Lee, A. Saraf, N. Shnidman, V. Strumpen, S. Amarasinghe, A. Agarwal. A 16-issue multiple-program-counter microprocessor with point-to-point scalar operand network. In *proceedings of the IEEE International Solid-State Circuits Conference*, February 2003.

H. Hoffmann, V. Strumpen, A. Agarwal. The Raw Microprocessor: Enabling Embedded Signal Processing on a General Purpose Computer Architecture. In *High Peformance Embedded Computing Workshop*, September 2002.

M. I. Gordon, W. Thies, M. Karczmarek, J. Lin, A. S. Meli, A. A. Lamb, C. Leger, J. Wong, H. Hoffmann, D. Maze, S. P. Amarasinghe. A stream compiler for communication-exposed architectures. In *Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems*, pages 291–303, May 2002.

M. B. Taylor, J. S. Kim, J. E. Miller, D. Wentzlaff, F. Ghodrat, B. Greenwald, H. Hoffmann, P. Johnson, J. Lee, W. Lee, A. Ma, A. Saraf, M. Seneski, N. Shnidman, V. Strumpen, M. Frank, S. P. Amarasinghe, A. Agarwal. The Raw Microprocessor: A Computational Fabric for Software Circuits and General-Purpose Programs. In *IEEE Micro*, vol. 22, no. 2, pages 25–35, 2002.

W. Thies, M. Karczmarek, M. I. Gordon, D. Maze, J. Wong, H. Hoffmann, M. Brown, S. P. Amarasinghe. A common machine language for grid-based architectures. In *SIGARCH Computer Architecture News*, vol. 30, no. 3, pages 13–14, 2002.

J. M. Lebak, J. Daly, H. Hoffmann, J. Kepner, J. Matlis, P. Richardson, E. Rutledge, G. Schrader. Software fault recovery for real-time signal processing on massively parallel computers. In *Proceedings of the SIAM Conference on Parallel Processing for Scientific Computing*, March 2001.

H. Hoffmann, J. Kepner, R. Bond. S3P: Automatic Optimized Mapping of Signal Processing Applications to Parallel Architectures. In *High Peformance Embedded Computing Workshop*, September 2001.

H. Hoffmann, J. Daly, J. Matlis, P. Richardson, E. Rutledge, G. Schrader. Achieving Portable Task and Data Parallelism on Signal Processing Architectures. In *High Peformance Embedded Computing Workshop*, September 2000.

Invited Talks

Henry Hoffmann. SEEC: A Self-aware Framework for Managing Goals and Constraints in Modern Computing Systems In *MIT Industrial Affiliates Program*, May 2012.

Henry Hoffmann. SEEC: A Self-aware Computational Model. In *High Peformance Embedded Computing Workshop*, September 2011.

Henry Hoffmann. Angstrom's Self-Aware Execution Model. In *Second ParalleX Execution Model Workshop* (PEMWS-2), April 2011.

Henry Hoffmann. Reducing Energy Consumption with Code Perforation. In *2nd Annual Conference on Computational Sustainability*, June 2010.

Yale Patt, Roger Espasa, Henry Hoffmann, Walid Najjar, Paolo Faraboshi (moderator). Panel Discussion: Heterogeneous vs. Homogeneous Computing. In *High Performance Embedded Architectures and Compilers*, January 2010.

Book Chapters

Michael B. Taylor, Walter Lee, Jason Miller, David Wentzlaff, Ian Bratt, Ben Greenwald, Henry Hoffmann, Paul Johnson, Jason Kim, James Psota, Arvind Saraf, Nathan Shnidman, Volker Strumpen, Matt Frank, Roderic Rabbah, Saman Amarasinghe, and Anant Agarwal. *Stream Multicore Processors*, chapter 14, pages 309–338. Springer, Dordrecht, The Netherlands, 2007.

Michael B. Taylor, Walter Lee, Jason E. Miller, David Wentzlaff, Ian Bratt, Ben Greenwald, Henry Hoffmann, Paul Johnson, Jason Kim, James Psota, Arvind Saraf, Nathan Shnidman, Volker Strumpen, Matt Frank, Saman Amarasinghe, and Anant Agarwal. *Tiled Multicore Processors*, chapter 1, pages 1–34. Springer, New York, NY, USA, 2009.

Publications Under Review

H. Hoffmann, M. Maggio, M. D. Santambrogio, A. Leva, A. Agarwal. The SEEC Framework for Self-Aware Computing. *In submission.*.

Patents

Nadya Travinin Bliss and Henry Hoffmann. Method and apparatus performing automatic mapping for a multi-processor system. Patent, July 2011. US 7983890 B2.

Professional Service

- Co-chair of 2nd International Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (co-located with DAC 2012)
- Program Committee for 9th International Conference on Embedded and Ubiquitous Computing 2011
- Reviewer for 2nd Annual Symposium on Cloud Computing 2011
- Co-chair of 1st International Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (co-located with ASPLOS 2011)
- Program Committee for 2nd Annual Workshop on Computer Architecture and Operating Systems co-design 2010
- Reviewer for International Symposium on Computer Architecture 2010
- Reviewer for International System-on-Chip Conference 2005

Awards

- Work on Self-aware computing named one of ten "World Changing Ideas" by Scientific American (Dec., 2011)
- Appointed MIT Lincoln Laboratory Doctoral Scholar (Declined appointment)
- Appointed MIT Lincoln Laboratory Masters Scholar
- Best Paper Award HPEC 2005
- Phi Beta Kappa
- Pi Mu Epsilon
- Received B.S. with Highest Honors and Highest Distinction
- Implementation of BDTI Wireless Communication Benchmark (OFDM) on Tilera TILEPro64 achieved highest performance on a programmable processor (as of 12/2011)

Teaching Experience

Massachusetts Institute of Technology

6.846 - Parallel Computing **Spring 2008**
Teaching Assistant

- Course teaches parallel applications, programming models, and architecture.
- Prepared and presented three lectures on: Tilera's TILE architecture, parallelizing video encoding, patterns of parallel programming
- Prepared and graded 5 homework assignments
- Put together and graded final project competition parallelizing a place-and-route application on the TILE processor
- Prepared dozens of pages of supplementary material on the TILE processor
- Held weekly office hours

University of North Carolina at Chapel Hill

COMP 14 - Introduction to Computer Science **Spring 1999**
Laboratory Assistant

- Course teaches introductory programming skills in C++.
- Designed and graded homework assignments
- Prepared and presented several lectures on C++ programming and software development
- Held regular office hours

Professional Experience

Self-employed, Cambridge, MA

Consultant on Multicore Application Development **February 2008 to present**

- Implemented BDTI OFDM Receiver Benchmark using 64 cores on Tilera TILE64 processor architecture
- Optimized single core performance of BDTI OFDM Receiver Benchmark on TILE64
- Optimized communication in parallel implementation of BDTI OFDM Receiver Benchmark on TILE64 and TILEPro64
- Designed parallel FFT for TILEPro64 architecture

Tilera Corporation, Westborough, MA

Design Engineer **December 2005 to February 2008**

- Designed programming abstraction to increase productivity of engineers developing parallel DSP code
- Contributed to design of architecture and programming model for a family of new parallel, multicore architectures
- Engaged with customers to understand their needs and how Tilera could better serve them
- Addressed technical and engineering questions on business development and sales calls
- Presented technical information on architecture, software, and applications to numerous customers
- Educated several customers on programming Tilera's hardware and parallel programming in general
- Ported many customer applications to Tilera hardware, including H.264 encoders, MPEG-2 encoders, 20+ DSP benchmarks, printing/imaging benchmarks, and wireless processing benchmarks

- Implemented scalable, real-time HD H.264 encoder executed on over 60 processors
- Implemented scalable, faster than real-time MPEG-2 encoder executed on over 60 processors

MIT Lincoln Laboratory, Lexington, MA

Associate Technical Staff **June 2003 to September 2004**

Assistant Technical Staff **July 1999 to June 2003**

- Designed and implemented algorithms, software, and run-time system for automatic parallelization of MATLAB programs
- Designed and implemented a C++ library for high performance parallel signal processing and scientific computing
- Designed and implemented algorithms, software, and run-time system for automatic parallelization of C++ digital signal processing programs
- Designed and implemented novel parallel algorithms for digital signal processing and linear algebra
- Evaluated emerging microarchitectures for use as embedded digital signal processing platforms
- Demonstrated to U.S. Navy viability of software and COTS solutions for real-time radar signal processing
- Implemented large-scale, parallel signal processing software for radar and sonar systems
- Mentored junior employees
- Prepared numerous technical presentations and documents

SAS Institute, Inc., Cary, NC

Summer Student **May 1998 to August 1998**

- Implemented C++ software to enable distribution of SAS databases
- Wrote test programs for existing SAS functionality
- Implemented an automated overnight regression test suite

References Available to Contact

Professor Anant Agarwal (e-mail: agarwal@csail.mit.edu; phone: +1-617-253-1448)
- Director, Computer Science and Artificial Intelligence Laboratory, Massachusetts Institute of Technology
- ◇ MIT CSAIL 32-G782, 32 Vassar Street, Cambridge, MA 02139
- ⋆ *Professor Agarwal is my graduate co-advisor and CTO of Tilera Corporation.*

Professor Srinivas Devadas (e-mail: devadas@mit.edu; phone: +1-617-253-0454)
- Professor, Massachusetts Institute of Technology
- ◇ MIT CSAIL 32-G844, 32 Vassar Street, Cambridge, MA 02139
- ⋆ *Professor Devadas is my graduate co-advisor.*

Professor Martin Rinard (e-mail: rinard@csail.mit.edu; phone: +1-617-258-6922)
- Professor, Massachusetts Institute of Technology
- ◇ MIT CSAIL 32-G828, 32 Vassar Street, Cambridge, MA 02139
- ⋆ *Professor Rinard is an advisor on the Code Perforation Project.*

Professor Marco D. Santambrogio (e-mail: santambr@elet.polimi.it; phone:+39-02-2399-3492)
- Assitant Professor, Politecnico di Milano
- ◇ Dipartimento di Elettronica e Informazione, Via Ponizo, 34/5, 20133 Milano, Italia
- ⋆ *Professor Santambrogio is a colleague and co-chair of the CHANGE workshop.*